REMARKS

Claims 5, 12, 18, 24, 35, 36, 38, 39, 41-44, 46-48 and 50-60 are pending in the present application. Claims 1-60 were examined. Claims 1-4, 6-11, 13-17, 19-23, 25-34, 37, 40, 45, and 49 have been cancelled by amendment.

In the office action mailed March 27, 2006 (the "Office Action"), the Examiner rejected claims 1-24 and 35-50 under 35 U.S.C. 112, second paragraph, as being indefinite. The Examiner further rejected claims 1, 5-6, 10, 11, 13, 17, 35, 38, 41-43, and 46 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,725,349 to Langendorf *et al.* (the "Langendorf patent"). The remaining claims were rejected under 35 U.S.C. 103(a) as being unpatentable over the Langendorf patent in view of U.S. Patent No. 6,947,050 to Jeddeloh (the "Jeddeloh patent"), admitted prior art ("APA"), and U.S. Patent No. 6,952,745 to Dodd *et al.* (the "Dodd patent"). The Examiner further commented on the number of references that have been disclosed through information disclosure statements ("IDSs").

With respect to the Examiner's comments on the IDSs, Applicant appreciates that the number of references that have been cited in the IDSs may place additional burden on the Examiner, but disagrees that the burden is undue. All of the references cited are ones Applicant has reason to believe may be relevant to the claims of this application. These references have all been properly cited in IDSs submitted in compliance with 37 C.F.R. 1.97 and 1.98. Accordingly, the IDSs shall be considered by the Examiner.

The Examiner suggests that the Applicant has not appropriately submitted the IDSs by failing to identify the most pertinent prior art and identify passages and figures of the cited references that are particularly relevant. However, despite the Examiner's assertion, this is not a duty imposed on the Applicant by the statutes, rules, or MPEP. If the Examiner is aware of any such requirement in 35 U.S.C., 37 C.F.R. or the MPEP, he is kindly requested to point out such requirement. As the Examiner may understand, if Applicant engages in picking and choosing which of these references to cite, Applicant runs the risk of being charged by a potential infringer with intentionally not citing any reference that is argued to be more material than those references chosen to be cited. Moreover, if Applicant engages in the practice of classifying the references by their degree of materiality, Applicant runs the risk of being charged by a potential infringer with failing to give references argued to be material a sufficiently high

rating of materiality for the purpose of misleading the Examiner. Either of these arguments can be the basis for a charge of inequitable conduct, which if established, renders a resulting patent unenforceable.

Finally, the Examiner has suggested in citing *Penn Yan Boats, Inc. v. Sea Lark Boats, Inc.* that Applicant may be attempting to "bury" pertinent prior art references within other disclosures of less relevant prior art. Applicant has not attempted to "bury" pertinent prior art with less relevant references in its submission of IDSs in the present application, and takes issue with the Examiner's suggestion that this may be the case. The references cited in the IDSs have been cited by Examiners in patent applications directed to subject matter related to the subject matter of the present patent application. The references have been cited in the present application out of an abundance of caution given the severe consequences of finding inequitable conduct by failing to cite relevant references.

Applicant requests the Examiner to consider the references cited in the previously submitted IDSs.

As previously mentioned, claims 1-4, 6-11, 13-17, 19-23, 25-34, 37, 40, 45, and 49 have been cancelled. The Examiner's rejection of these claims is now moot.

With respect to the claim rejections under 35 U.S.C. 112, second paragraph, claims 5, 35, 38, 41, 43, 44, and 47 have been amended to remove reference to "high-speed." Consequently, the Examiner's rejection of the claims under 35 U.S.C. 112, second paragraph, should be withdrawn.

As previously mentioned, the Examiner rejected claims 5, 35, 38, 41-43, and 46 under 35 U.S.C. 102(e) as being anticipated by the Langendorf patent.

The Langendorf patent describes a memory controller that supports both standard page mode dynamic random access memory ("DRAM") and extended data-out ("EDO") DRAM. As described in the Background of the Langendorf patent, conventional memory systems that mix page mode and EDO DRAM typically have reduced memory performance because only one of the two timing protocols (i.e., either page mode or EDO) can be used. However, the memory controller proposed in the Langendorf patent is capable of controlling both types of memory when used together in main memory. As shown in Figure 2 of the Langendorf patent, the memory controller 105 is coupled to a processor 102 and coupled to main memory 103. The

control signals, represented by RAS# 215 and CAS# 220, are coupled to page mode DRAM 225 and EDO DRAM 230, both of which are included in the main memory 103.

Figure 3 illustrates the DRAM controller 105 in greater detail. Configuration registers 300 store information identifying the type of DRAM corresponding to each memory bank of the main memory 103. The information loaded into the configuration registers 300 can be provided by the system BIOS. During access of a bank of memory of the main memory 103, a memory address is decoded by a bank decoder 310 and the corresponding bank of memory is identified. Information of the identified bank of memory is provided to a select multiplexer 320, which compares that information with the information loaded in the configuration registers 300. The type of DRAM of the corresponding bank of memory to be accessed can then be identified as either page mode or EDO. Based on the type of DRAM, the select multiplexer 320 controls a CAS# state machine 330 to provide CAS# signals according to the appropriate timing. In this manner, memory accesses to page mode DRAM is handled using different timing than memory access to EDO DRAM.

Claims 35, 38, and 43 are patentably distinct from the Langendorf patent because the Langendorf patent fails to disclose the combination of limitations recited by the respective claim.

For example, with respect to claim 35, the Langendorf patent fails to disclose memory hub having an electrically programmable non-volatile memory, and also first and second configuration paths that couple the electrically programmable non-volatile memory to a link interface and a memory controller, respectively. The Langendorf patent further fails to disclose a local serial bus also included in the memory hub that is coupled to the electrically programmable non-volatile memory to provide a host system access thereto.

The Examiner argues that the electrically programmable non-volatile memory recited in claim 35 is disclosed by the system BIOS, which is described as providing information to the configuration registers 300. However, the system BIOS, shown in Figure 1 as read only memory ("ROM") 106, is not included on a memory hub. The ROM 106 is merely coupled to a bus 101. Figure 1 illustrates main memory 103 as being a separate functional block that is separately coupled to the bus 101. In contrast, claim 35 claims a memory hub that includes, among other things, an electrically programmable non-volatile memory.

Moreover, as previously discussed, the Langendorf patent fails to disclose the first and second configuration paths, as well as the local serial bus recited in claim 35. The ROM 106 described in the Langendorf patent is coupled to the bus 101, and at best, is accessed by the DRAM controller 105 through the bus 101. Claim 35 recites that the memory hub includes a memory controller that is coupled to the electrically programmable non-volatile memory through the second configuration path. Claim 35 further recites that the memory hub includes a local serial bus that provides the host system access to the electrically programmable non-volatile memory. The recitation of the second configuration path and the local serial bus clarify that the memory controller can access the non-volatile memory without using the same bus as a host system. That is, the memory controller of claim 35 is provided with separate access to the non-volatile memory from the host system.

Based on the description of the memory controller and the computer system described in the Langendorf patent, separate access to the non-volatile memory, as recited in claim 35, is not disclosed. Nor is the structure of the memory hub of claim 35 contemplated, since the Langendorf patent is directed to a DRAM controller 105 that is capable of supporting both page mode and EDO DRAM mixed together in main memory 103. The DRAM controller 105 accesses main memory 103 generally, and is not included in a memory hub for a hub-based memory sub-system. The DRAM controller 105 is designed to support different types of DRAM that can be included in the main memory 103, rather than being associated with any particular memory module in main memory. As a result, having both a configuration path through which the memory controller 103 has access to the non-volatile memory and a local serial bus through which a host system has access to the non-volatile memory is not contemplated in the Langendorf patent.

Claims 38 and 43 recite limitations similar to those previously discussed with respect to claim 35. For example, claim 38 recites a memory sub-system that includes at least one memory module, each memory module having a memory hub that includes, among other things, a configuration memory coupled to a local serial bus that provides access to a host computer system and also a memory controller coupled to the configuration memory through a configuration path. Claim 43 recites a memory module having a memory hub that includes a local serial bus coupled to a electrically erasable programmable non-volatile memory and further

includes a configuration path that couples a memory controller to the electrically erasable programmable non-volatile memory. As previously discussed with respect to claim 38, the Langendorf patent fails to disclose these limitations. Moreover, the Langendorf patent is directed to a memory controller 105 that can support both page mode and EDO DRAM included in main memory 103. The memory controller 105 is for accessing the main memory 103 generally, unlike claims 38 and 43, which recite memory modules each having a respective memory hub.

For the foregoing reasons, claims 35, 38, and 43 are patentably distinct from the Langendorf patent. Claim 5, which depends from claim 35, claims 41 and 42, which depend from claim 38, and claim 46, which depends from claim 43, are also patentably distinct from the Langendorf patent based on their dependency from a respective allowable base claim. Therefore, the Examiner's rejection of claims 5, 35, 38, 41-43, and 46 under 35 U.S.C. 102(e) should be withdrawn.

Claim 47 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Langendorf patent in view of the Jeddeloh patent.

Claim 47 is patentable over the Langendorf patent in view of the Jeddeloh because the combined teachings of the cited references fail to teach or suggest the combination of limitations recited by claim 47. Claim 47 recites a processor-based system including a memory module that has a memory hub similar to that recited in claim 35.

The Examiner has cited the Jeddeloh patent as teaching a system controller as recited in claim 47. Even if it is assumed for the sake of argument that the Examiner's characterization of the Jeddeloh patent is accurate, it fails to make up for the deficiencies of the Langendorf patent as previously discussed with respect to claims 35, 38, and 43. More specifically, the Jeddeloh patent fails to describe a memory hub that includes a first and second configuration path and a local serial bus, as recited in claim 47.

For the foregoing reasons, claim 47 is patentable over the Langendorf patent in view of the Jeddeloh patent, and therefore, the rejection of claim 47 under 35 U.S.C. 103(a) should be withdrawn.

Claims 51 and 57 have been rejected by the Examiner under 35 U.S.C. 103(a) as being unpatentable over the Langendorf patent, and alternatively, unpatentable over the Langendorf patent in view of the Jeddeloh patent.

The Examiner argues that although Langendorf does not disclose a plurality of non-volatile memories each copying to a respective controller, it would have been obvious to those ordinarily skilled in the art to use the teachings of Langendorf to do so. *See* the Office Action at pages 5-6. The Examiner's argument, however, does not take into consideration the teachings of the Langendorf in its entirety. As previously discussed, the Langendorf patent is directed to a memory sub-system having a memory controller that supports both page mode and EDO DRAM used together in the main memory. The purpose of having such a memory controller is so that the memory controller can take advantage of the page mode and EDO functions of the different DRAM (likely in the form of memory modules populated with either page mode or EDO DRAM) that are present in main memory. In this manner, the memory controller is equipped to efficiently control the memory in main memory, regardless of the combination of the particular type of DRAM utilized.

Using the memory controller as described in the Langendorf patent as a "memory hub" for a memory module is unlikely since page mode and EDO DRAM are typically not mixed together on a memory module. Consequently, there is no real motivation to incur the additional costs of including a memory controller that is capable of supporting both page mode and EDO DRAM on the module when there is only one type of DRAM used. Moreover, even if the teachings of Langendorf are "scalable," as suggested by the Examiner, *see* the Office Action at pages 5-6, the result of scaling the teachings would be to scale the memory sub-system to have multiple memory controllers to control multiple memory domains. Each domain would include both page mode and EDO DRAM which are controlled by a respective memory controller. Even with scaling the memory sub-system, there would be no reason to also include multiple ROMs 106 since all of the memory configuration information is stored in the ROM 106, which can then provided to the memory controllers. It is unlikely that an artisan would want to increase the cost and the complexity of a memory sub-system by including additional ROMs 106 when only one ROM will do.

The Examiner argues in the alternative that the teachings of the Jeddeloh patent render claims 51 and 57 obvious. In particular, the Examiner argues that the Jeddeloh patent discloses a system having multiple processors and multiple memory controllers, each having registers loaded from non-volatile memory. *See* the Office Action at page 6. The Jeddeloh patent describes an embodiment where a GART table 210 is implemented by an initialization BIOS. *See* col. 7, lines 7-10. However, there is no suggestion that increasing the number of initialization BIOS would be beneficial or desirable. In fact, the Jeddeloh patent describes another embodiment that completely avoids the use of initialization BIOS for implementing the GART tables. See col. 7, lines 10-13. Given this alternative to using initialization BIOS, there is no motivation to add cost and complexity to the main memory by including multiple non-volatile memory.

A set forth above, the Examiner has failed to establish a *prima facie* case of obviousness by failing to provide sufficient motivation to modify the teachings of the Langendorf patent and the Jeddeloh patent. Consequently, the rejection of claims 51 and 58 under 35 U.S.C. 103(a) cannot be maintained and should be withdrawn.

Pending dependent claims 36, 39, 44, 48, 50, 52-56, and 58-60 have been rejected under 35 U.S.C. 103(a) as being unpatentable over various combinations of the Langendorf patent, the Jeddeloh patent, the Dodd patent, and the APA. These claims are patentable based on their dependency on a respective allowable base claim. Therefore, the rejection of claims 36, 39, 44, 48, 50, 52-56, and 58-60 under 35 U.S.C. 103(a) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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